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EXAMINER	
ZHOU, YONG	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,874	LU ET AL.	
	Examiner	Art Unit	
	Yong Zhou	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,19 and 20* is/are allowed.

6)☒ Claim(s) *21-28 and 30-37* is/are rejected.

7)☒ Claim(s) *29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 28 and 33 are objected to because of the following informalities:

Regarding claim 28, there should be a period (.) at the end of the claim, not semicolon.

Regarding claim 33, a period (.) is missing at the end of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 30 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30 recites the limitation "relabeling any internal". It is believed to be "relabeling any internal ports".

Claim 35 recites the limitation "each switching network belongs to". It is believed to be "each switching element belongs to".

Appropriate correction is required.

4. **Claims 1, 2, 19 and 20** are allowed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 21-28, 34-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Prasad, Sharat C. (US 6,049,542), referred to herein as Prasad.

Regarding claim 21, Prasad teaches a method of reconfiguring (col. 1, lines 9-11) comprising:

designating a scalable switching network having a plurality of stages of switching elements, a plurality of internal ports, a plurality for external ports, and a plurality of internal connections, wherein the internal ports and external ports are coupled to one of the switching elements and the internal connections are coupled to two of the internal ports (Fig. 4, col. 2, lines 39-46, wherein the scalable switch fabric architecture comprises multiple internal and external ports, multiple switching elements and multiple internal connections);

providing a post-reconfiguration architecture (Fig. 4);

adding new hardware comprising a plurality of internal ports as defined by the post- reconfiguration architecture (Fig. 4, #301 is the new hardware for new core stage and it comprises multiple internal ports);

deactivating any external ports connected to any hardware not present in the post- reconfiguration architecture (Fig. 4, ports of #113-118 and #133-138, col. 7, lines 42-47, wherein switches 113-118 and 133-138 were unconnected prior the replacement, therefore their exports were deactivated);

assigning to each internal port a corresponding port defined by the post-reconfiguration architecture (Fig. 4, #111-112, #301, #131-132, wherein output port 1 of switch element #111 is assigned to input port 1 of switch #411 in the replacement core #301, output port 2 of #111 to input port 1 of #415, .., input port 3 of #132 to output port 1 of #436, input port 4 of #132 to output port 1 of #438);

rewiring any internal port on the basis of the post-reconfiguration architecture (Fig. 3, Fig. 4, #121, #122, #301, col. 7, lines 28-30, wherein the new core stage #301 replaces the second stage #121-122 and output ports of #111-112 are re-connected through #301 to #131-132 and the original second stage is inactive);

removing any hardware not present in the post-reconfiguration architecture (Fig. 3, #121-122, Fig. 4, col. 7, lines 31-32, wherein the original switch elements #121-122 not included in the post-reconfiguration are removed).

Regarding claim 22, Prasad further teaches that said new hardware further comprises a plurality of new external ports (Fig. 4, #301, col. 8, lines 33-34, wherein

new core stage has plurality external ports (externally symmetric)), and further comprising:

activating the plurality of new external ports (Fig. 4, #301, col. 7, line 28, col. 8, lines 33-34, wherein the export ports of the new core are activated in the process of core stage replacement).

Regarding claim 23, Prasad further teaches that said new hardware comprises at least one new stage of switching elements (Fig. 4, the new hardware # 301 has three stages).

Regarding claim 24, Prasad further teaches that said new hardware comprises at least one new switching element (Fig. 4, the new hardware # 301 has twenty four switching elements, #411-418, #421-428, #431-438).

Regarding claim 25, Prasad further teaches that said new hardware comprises at least one new port to at least one of the switching elements (Fig. 4, each switching element in the new hardware # 301 has four input ports and four output ports).

Regarding claim 26, Prasad further teaches that any hardware not present in the post- reconfiguration architecture comprises either at least one switching element or at least one new port to at least one of the switching elements (Fig. 3, Fig. 4, switch elements #121-122 are not present in the post-configuration architecture and they have 4 input ports and four output ports).

Regarding claim 27, Prasad further teaches:

pre-connecting any internal port on the basis of the post-reconfiguration architecture (Fig. 4, #301, col. 8, lines 25-30, wherein the switching elements in the three stages of the new core stage hardware are pre-connected).

Regarding claim 28, Prasad further teaches that the pre-connecting comprises:

selecting a pre-connection port of the plurality of internal ports that is not coupled to any connection and having assigned a corresponding port that is not coupled to any connections (Fig. 4, #411, #422, col. 8, lines 25-30, wherein for one of the pre-connections, the output port 3 of #411 and corresponding input port 1 of #422 are selected); and

connecting the pre-connection port to the corresponding port assigned to the pre-connection port by coupling a first connection to the pre-connection port and to the corresponding port assigned to the pre-connection port connections (Fig. 4, #411, #422, col. 8, lines 25-30, wherein for one of the pre-connections, the output port 3 of #411 and corresponding input port 1 of #422 are selected).

Regarding claim 34, Prasad further teaches that the scalable switching network is a multi-stage interconnection network (Fig. 3 #300, Fig. 4, #400, col. 7, lines 23-25, wherein the scalable switching network #300 and #400 contain three or more stages).

Regarding claim 35, Prasad further teaches that the scalable switching network comprises a plurality of columns wherein each switching element belongs to one of the plurality of stages and one of the plurality of columns, and wherein internal connections either couple ports in adjacent stages or couple ports in adjacent columns (Fig. 4, wherein the scalable switch fabric comprises multiple rows (corresponding to the

claimed "columns"), each switching element belongs to one of stages and one of rows, and the internal connections couple two ports in adjacent stages).

Regarding claim 36, Prasad teaches a method of reconfiguring (col. 1, lines 9-11) comprising:

designating a scalable switching network for downgrading having a plurality of stages of switching elements, a plurality of internal ports, a plurality for external ports, and a plurality of internal connections, wherein the internal ports and external ports are coupled to one of the switching elements and the internal connections are coupled to two of the internal ports (Fig. 4, col. 2, lines 39-46, wherein the scalable switch fabric architecture comprises multiple internal and external ports, multiple switching elements and multiple internal connections; the scalable switch fabric can be scaled down or scaled up) ;

providing a post-reconfiguration architecture (Fig. 4);

deactivating any external ports connected to any hardware not present in the post- reconfiguration architecture (Fig. 4, ports of #113-118 and #133-138, col. 7, lines 42-47, wherein switches 113-118 and 133-138 were unconnected prior the replacement, therefore their exports were deactivated);

assigning to each internal port a corresponding port defined by the post-reconfiguration architecture (Fig. 4, #111-112, #301, #131-132, wherein output port 1 of switch element #111 is assigned to input port 1 of switch #411 in the replacement core #301, output port 2 of #111 to input port 1 of #415, .., input port 3 of #132 to output port 1 of #436, input port 4 of #132 to output port 1 of #438);

pre-connecting any internal port on the basis of the post-reconfiguration architecture (Fig. 4, #301, col. 8, lines 25-30, wherein the switching elements in the three stages of the new core stage hardware are pre-connected);

rewiring any internal port on the basis of the post-reconfiguration architecture (Fig. 3, Fig. 4, #121, #122, #301, col. 7, lines 28-30, wherein the new core stage #301 replaces the second stage #121-122 and output ports of #111-112 are re-connected through #301 to #131-132 and the original second stage is inactive); and

removing any hardware not present in the post-reconfiguration architecture (Fig. 3, #121-122, Fig. 4, col. 7, lines 31-32, wherein the original switch elements #121-122 not included in the post-reconfiguration are removed).

Regarding claim 37, Prasad further teaches:

adding new hardware comprising a plurality of internal ports and a plurality of new external ports as defined by the post-reconfiguration architecture (Fig. 4, #301, col. 8, lines 33-34 wherein the new hardware for new core stage and it comprises multiple internal ports and external ports);

activating the plurality of new external ports (Fig. 4, #301, col. 7, line 28, col. 8, lines 33-34, wherein the export ports of the new core are activated in the process of core stage replacement).

Allowable Subject Matter

7. **Claim 29** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad in view of Huang, Alan (US 5,841,775), referred to herein as Huang.

Regarding claims 30-32, Prasad teaches the limitations of claim 21.

Prasad does not specifically teach re-labeling the internal ports on the basis of the post-configuration architecture.

Huang teaches that the mapping interconnect can be altered via relabeling the ports assuming all ports on the switching elements are equivalent (col. 15, lines 15-18).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Huang into the Prasad invention to re-label the ports to alter the mapping interconnect in the process of reconfiguring the scalable switch fabric.

Regarding claim 33, Prasad teaches the limitations of claim 21.

Prasad does not specifically teach that the scalable switching network is a redundant blocking compensated cyclic group multi-stage network.

Huang teaches a redundant blocking compensated cyclic group multi-stage network (col. 2, line 54, col. 11, lines 61-66).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Huang into the Prasad invention to include the redundant blocking compensated cyclic group multi-stage network in the scalable switch reconfiguration process.

Response to Arguments

10. Applicant's arguments filed December 26, 2007 have been fully considered.

Regarding the double patenting rejection to claims 1 and 2, Applicant argues that not every element in claim 1 of the present application is present in the claims of patent 7,123,612, although two claim sets share common elements. Applicant's arguments are persuasive. Therefore, claims 1 and 2 are allowed. The newly added claims 19 and 20 that are dependent on claim 1 are also allowed.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yong Zhou whose telephone number is (571)270-3451. The examiner can normally be reached on Monday - Friday 8:00am - 5:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag G. Shah can be reached on (571) 272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yong Zhou

March 17, 2008

/Chirag G Shah/
Supervisory Patent Examiner, Art Unit 2619